Amendments to the Specification:

Please replace the two paragraphs on page 3, line ~~16~~ 17 to page 4, line ~~7~~ 4 of the specification with the following two new paragraphs: YCC 3/13/07

--Figure 1 illustrates a first embodiment of the invention. A first expression of the first embodiment is for a memory module 10. The memory module 10 includes read only memory (ROM memory) cells 12 and a non-ROM to ROM interface ~~14~~ (such as an erasable programmable read only memory [EPROM] to ROM interface such as a Flash to ROM interface 18) operatively connected to the ROM memory cells 12. In one application, the memory module 10 is used in a computer device having a non-ROM memory control which expects to communicate with a corresponding non-ROM memory module.

~~In one example, the non-ROM to ROM interface 14 is an erasable programmable read only memory (EPROM) to ROM interface 16. In one variation, the EPROM to ROM interface is a Flash to ROM interface 18.~~ In one modification, the Flash to ROM interface 18 is a serial interface. In one implementation, the Flash to ROM interface 18 has connections for a Flash clock transmission line 20 (labeled as CLK), a Flash serial input transmission line 22 (labeled as SI), a Flash serial output transmission line 24 (labeled as SO), a Flash chip select transmission line 26 (labeled as CS), and a Flash reset transmission line 28 (labeled as RESET). During operation of the Flash serial input transmission line 22, the Flash serial input transmission line 22 transmits a command selected from the group consisting of a status (i.e., status read) command, a read (i.e., data read) command, and a write (i.e., data write) command to the Flash to ROM interface 18. In one design, the Flash to ROM interface 18 passes through the status and read commands to the ROM memory cells 12 but only indicates a ready status without passing through the write command to the ROM memory cells 12.--

Please replace the two paragraphs on page 6, lines ~~8~~ page 7, line 2 to ~~33~~ of the specification with the following two new paragraphs: YCC 3/13/07

--A second expression of the first embodiment of the invention of Figure 1 is for a printer assembly 30. The printer assembly 30 includes a printer-controller ASIC 32, a memory module

10, and a transmission cable 34. The printer-controller ASIC 32 has a non-ROM memory control ~~36~~ (such as an EPROM memory control such as a Flash memory control 40. The memory module 10 includes ROM memory cells 12 and a non-ROM to ROM interface ~~14~~ (such as an erasable programmable read only memory [EPROM] to ROM interface such as a Flash to ROM interface 18 operatively connected to the ROM memory cells 12. The transmission cable 34 is operatively connected to the non-ROM memory control 36 of the printer-controller ASIC 32 and the non-ROM to ROM interface 14 of the memory module 10.

In one example, the non-ROM memory control 36 of the printer-controller ASIC 32 is an EPROM memory control 38, and the non-ROM to ROM interface 14 is an EPROM to ROM interface 16. In one variation, the EPROM memory control 38 of the printer-controller ASIC 32 is a Flash memory control 40, and the EPROM to ROM interface is a Flash to ROM interface 18. In one modification, the Flash memory control 40 is a serial memory control, and the Flash to ROM interface 18 is a serial interface. The serial Flash to ROM interface makes it appear to the printer-controller ASIC that a Flash memory module (having a serial Flash interface and Flash memory cells) is attached to the serial Flash memory control of the printer-controller ASIC when in reality the memory module 10 (having the serial Flash to ROM interface and the ROM memory cells) is attached to the serial Flash memory control of the printer-controller ASIC. In one implementation, the transmission cable 34 includes a Flash clock transmission line 20, a Flash serial input transmission line 22, a Flash serial output transmission line 24, a Flash chip select transmission line 26, and a Flash reset transmission line 28. During operation of the printer-controller ASIC 32, the Flash control 40 transmits through the Flash serial input transmission line 22 a command selected from the group consisting of a status command, a read command, and a write command to the Flash to ROM interface 18. In one design, the Flash to ROM interface 18 passes through the status and read commands to the ROM memory cells 12 but only indicates a ready status without passing through the write command to the ROM memory cells 12.--

Please replace the two paragraphs on page 7, line 6 to page 8, line 6 of the specification with the following two new paragraphs: ycc 3/13/07

--A first method of the invention is for storing a computer code for a printer-controller ASIC 32 having a non-ROM memory control ~~36~~ and is shown in Figure 2. The first method includes steps a) and b). Step a) is labeled in block 42 of Figure 2 as "Store Non-Final Code In First Memory Module". Step a) includes storing non-final versions of the computer code in a first memory module, wherein the first memory module has non-ROM memory cells and a non-ROM interface, and wherein the non-ROM interface is operatively connected to the non-ROM memory control ~~36~~ of the printer-controller ASIC 32 and to the non-ROM memory cells of the first memory module. Step b) is labeled in block 44 of Figure 2 as "Store Final Code In Second Memory Module". Step b) includes storing the final version of the computer code in a second memory module (such as memory module 10), wherein the second memory module has a non-ROM to ROM interface ~~(such as non-ROM to ROM interface 14)~~ and ROM memory cells (such as ROM memory cells 12), wherein the non-ROM to ROM interface is operatively connected to the non-ROM memory control ~~36~~ of the computer-controller ASIC 32 and to the ROM memory cells of the second memory module, and wherein the second memory module physically replaces the first memory module.

In one example, the non-ROM memory control ~~36~~ of the printer-controller ASIC 32 is an EPROM memory control ~~38~~, the first memory module has EPROM memory cells and an EPROM interface, and the second memory module has an EPROM to ROM interface. In one variation, the EPROM memory control ~~38~~ of the ASIC 32 is a Flash memory control 40, the first memory module has Flash memory cells and a Flash interface, and the second memory module has a Flash to ROM interface. In one modification, the Flash memory control 40 is a serial memory control, the Flash interface of the first memory module is a serial interface, and the Flash to ROM interface of the second memory module is a serial interface. In one implementation, the Flash to ROM interface has connections for a Flash clock transmission line 20, a Flash serial input transmission line 22, a Flash serial output transmission line 24, a Flash chip select transmission line 26, and a Flash reset transmission line 28. During operation of the Flash serial input transmission line 22, the Flash serial input transmission line 22 transmits a command selected from the group consisting of a status command, a read command, and a write command to the Flash to ROM interface 18. In one design, the Flash to ROM interface passes through the status and read commands to the ROM memory cells but only indicates a ready

status without passing through the write command to the ROM memory cells.--